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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
ALCALA, JOSE H

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/471,071	JIANG, TONGBI	
	Examiner	Art Unit	
	Jose H Alcala	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This non-final rejection is in response to amendment filed on 1/29/03.

Drawings

2. The corrected or substitute drawings were received on 1/29/03. These drawings are acceptable.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 8-23, 25-28 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The specific materials of the die attach layer which are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). For example, in claim 8, the claim recites that the die attach layer has a thermal expansion coefficient of less than about 106 ppm/°C, but there is no place in that claim or in the disclosure what material has that property.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Khandros et al. As best understood by the examiner:

7. Regarding Claim 25, Khandros teaches an integrated circuit package, comprising: a flexible substrate (reference number 66); a chip (reference number 20); a plurality of conductive terminals (reference number 70) on the substrate; a plurality of conductive leads (reference number 48) electrically connecting the conductive terminals to the chip; and a compliant material (reference number 58) between the chip and the substrate. In addition, Khandros teaches that the compliant material is an elastomer compliant layer, therefore it is inherent that it can have a modulus of elasticity of less than about 126 ksi and a coefficient of thermal expansion of less than about 106 ppm/°C.

Regarding Claim 26, DiStefano teaches that the plurality of conductive terminals includes an array of solder balls (reference number 70).

Regarding Claim 27, DiStefano teaches that the plurality of conductive leads includes TAB leads (column 13, line 35).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 8-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano et al. (US Patent No. 5,821,608). As best understood by the examiner:

Regarding Claim 8, DiStefano teaches an integrated circuit package, comprising: a die (reference number 10); a die attach layer over the die (reference number 80'); and an array of solder balls (reference number 40) over the die attach layer. DiStefano further teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material with a higher thickness to compensate for thermal mismatch.

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient of about 106 ppm/°C, in order to compensate for thermal mismatch in the package, and since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 9, DiStefano teaches a flexible tape (reference number 50) connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

Regarding Claim 10, DiStefano teaches that the die attach layer has a thickness of between about 5 and 7 mils (column 6, lines 9-11).

Regarding Claim 11, DiStefano fails to explicitly teach that the die attach layer is an epoxy modified with elastomeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the die attach layer

of a thermoplastic or thermoset material, which could be an epoxy modified with elastomeric material, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. See In re Leshin, 125 USPQ 416.

Regarding Claim 12, DiStefano teaches that the array is a ball grid array (See Figure 1A).

Regarding Claim 13, DiStefano teaches that the array is a tape ball grid array (See Figure 1A).

Regarding Claim 14, DiStefano teaches that the array is a micro ball grid array (See Figure 1A).

Regarding Claim 15, DiStefano teaches an integrated circuit package, comprising: a die (reference number 10); a die attach layer over the die (reference number 80'); and an array of solder balls (reference number 40) over the die attach layer. DiStefano further teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material with a higher thickness to compensate for thermal mismatch.

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C, and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient of about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi, in order to compensate for thermal mismatch in the package, and

since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges, or discovering an optimum value of a result effective variable involve only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980), and In re Aller, 105 USPQ 233.

Regarding Claim 16, DiStefano teaches a flexible tape (reference number 50) connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

Regarding Claim 17, DiStefano teaches a first level integrated circuit package comprising: a first level package including a chip (reference number 10); an array of solder balls (reference number 40), an adhesive layer (reference number 80) between the chip and the array of solder balls, and a flexible tape (reference number 50) connecting the array to the chip wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip. The limitation that the array of solder balls is: "for connecting the first level package to a second level package", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 200 ppm/°C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient of about 200 ppm/°C, in order to compensate for

thermal mismatch in the package, and since it has been held that discovering an optimum value of a result effective variable, involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 18, DiStefano teaches that the tape connects the array to the chip using μBGA technology (See Figure 1a).

Regarding Claim 19, DiStefano teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material with a higher thickness to compensate for thermal mismatch.

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 150 ppm/°C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient of about 150 ppm/°C, in order to compensate for thermal mismatch in the package, and since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 20, DiStefano teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material with a higher thickness to compensate for thermal mismatch.

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 100 ppm/°C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient of about 100 ppm/°C, in order to compensate for

thermal mismatch in the package, and since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 21, DiStefano teaches a first level integrated circuit package comprising: a first level package including a chip (reference number 10); an array of solder balls (reference number 40), an adhesive layer (reference number 80) between the chip and the array of solder balls, and a flexible tape (reference number 50) connecting the array to the chip wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip. The limitation that the array of solder balls is: "for connecting the first level package to a second level package", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 200 ppm/°C, and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient of about 200 ppm/°C and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi, in order to compensate for thermal mismatch in the package, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges, or discovering an optimum value of a result

effective variable, involve only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980), and In re Aller, 105 USPQ 233.

Regarding Claim 22, DiStefano teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material with a higher thickness to compensate for thermal mismatch.

DiStefano fails to explicitly teach that the die attach layer has a modulus of elasticity of greater than about 50 ksi. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a modulus of elasticity of greater than about 50 ksi, in order to compensate for thermal mismatch in the package, and since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 23, DiStefano teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material with a higher thickness to compensate for thermal mismatch.

DiStefano fails to explicitly teach that the die attach layer has a modulus of elasticity of greater than about 100 ksi. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a modulus of elasticity of greater than about 100 ksi, in order to compensate for thermal mismatch in the package, and since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

10. Claim 28, is rejected under 35 U.S.C. 103(a) as being unpatentable over Khandros et al. (US Patent No. 5,148,265). As best understood by the examiner:

Regarding Claim 28, Khandros teacheas all the elements as stated supra for claim 25, but fails to explicitly teach that the flexible substrate is a polyimide. DiStefano further teaches the desirability of using polyimide for the compliant layer in order to compensate for thermal mismatch. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the flexible substrate of a polyimide, in order to compensate for thermal mismatch, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. See In re Leshin, 125 USPQ 416.

Response to Arguments

11. Applicant's arguments with respect to claims 8-23,25-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention or some similar arrangements of the elements: Khandros et al.

(US Patent No. 5,148,266), Takahashi et al. (US Patent No. 6,576,984) and DiStefano et al. (US Patent No. 5,536,909).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
July 21, 2003

John B. Vigushin
Examiner
AU 2827

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800